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11-27-01

500.40681X00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): T. Ohyanagi et al.
Serial No.: Not yet assigned
Filed: September 28, 2001
For: FIELD EFFECT TRANSISTOR AND SEMICONDUCTOR
DEVICE MANUFACTURING METHOD
Group:
Examiner:

jc714 U.S. PTO
09/28/01
09/28/01

INFORMATION DISCLOSURE STATEMENT
UNDER 37 CFR 1.97 & 1.98

Assistant Commissioner
for Patents
Washington, D.C. 20231

September 28, 2001

Sir:

In the matter of the above-identified application, applicants are submitting herewith copies of the documents listed in the attached form equivalent to Form PTO-1449 for the Examiner's consideration.

This information disclosure statement is being submitted with the new application.

Each of the documents listed on the attached form equivalent to Form PTO-1449 is in the English language.


It is respectfully requested that this information disclosure statement be considered by the Examiner.

Please charge any shortage in the fees due in connection

with the filing of this paper, including extension of time fees, to the deposit account of Antonelli, Terry, Stout & Kraus Deposit Account No. 01-2135 (500.40681X00) please credit any excess fees to such deposit account.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP



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Form PTO-1449 INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DKT. NO. 500.40681X00	SERIAL NO. Not yet assigned
	APPLICANT T. Ohyanagi et al.		
	FILING DATE Sept. 28, 2001	GROUP	

U.S. PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date
AA						
AB						
AC						
AD						

FOREIGN PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Country	Class	Subclass	Translation / Abstract	
						Yes	No
AM	A-11-121742	4/30/99	Japan			X	
AN	A-05-129602	5/25/93	Japan			X	
AO	A-07-086580	3/31/95	Japan			X	
AP	A-05-110080	4/30/93	Japan			X	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

AU	IEDM 89, "Asymmetrical Halo Source GOLD drain (HS-GOLD) Deep Sub-half Micron n-MOSFET Design for Reliability and Performance" pp. 617-620
AV	
AW	
AX	
AY	
AZ	
Examiner	Date Considered

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 09/28/01
